REMARKS

Favorable reconsideration of this application as amended is respectfully requested.

Claims 3, 4, and 5 have been amended to overcome the rejection under 35 U.S.C. § 112, second paragraph. The term "area occupation rate" is used in the specification. See e.g., page 42, line 15. The term refers to the percentage of an area occupied by wiring. The percentage figures recited in Claims 4 and 5 designate variations in the area occupation rates, not the occupation rates themselves.

The rejections under 35 U.S.C. § 102(b) and § 103(a) based on Yamaha (6,297,563) or Yamaha in view of Furuhata (2002/0121701) or Wong (2002/0019082) are respectfully traversed, particularly as those rejections relate to the claims now presented.

Independent Claim 1 now recites, inter alia, semiconductor elements formed on a substrate; plural electrode pads arranged over said semiconductor elements; and a wiring layer arranged over said semiconductor elements, said wiring layer being arranged below said plural electrode pads, wherein area occupation rates of

wiring arranged in areas of respective planar regions of the plural electric pads are substantially uniform.

As described in Applicants' specification at page 1, line 21 to page 2, line 1 and at page 13, lines 7-17, a technique or system is now being adopted in which electrode pads are arranged in a more inner region of a semiconductor chip where elements and wirings are arranged (i.e., an active region). By virtue of Applicants' invention, the levels or heights at the upper surfaces of a plurality of electrode pads within a main surface of a semiconductor chip can be made substantially uniform. Because bonding failure can be reduced between the electrode pads of the semiconductor chip and the wiring of a packaging body for packaging the semiconductor chip, assembling defects can be reduced when the semiconductor chip is packaged. See Applicants' specification, page 57, line 3, to page 58, line 10.

The invention recited in Claim 1 is neither taught nor suggested by the prior art, including Yamaha or Yamaha in combination with the secondary references relied upon in the rejections.

As shown in Figs. 1 and 2 of Yamaha, Yamaha discloses a bonding pad 32b and bottom wiring layers 20b, 14b formed

under the bonding pad 32b. As shown in Figs. 1 and 3, however, the bonding pad 32b and the bottom wiring layers 20b, 14b are arranged in a bonding pad area B around an inner wiring area A. In other words, the bottom wiring layers 20b, 14b are not formed over semiconductor elements (and are not formed for integrated circuits). To the contrary, in the present invention, wirings are formed over semiconductor elements (for integrated circuits), which permits reduction of the area of a semiconductor chip.

The deficiencies of Yamaha with regard to the invention recited in Claim 1 are not cured by the secondary references. Accordingly, Claim 1 and the claims dependent thereon should be allowed.

New independent Claim 45 recites a semiconductor device comprising a semiconductor element formed on a substrate; a wiring layer formed over said semiconductor element and having wiring connected to said semiconductor element; and a pad formed over said wiring layer. As further recited, in said wiring layer an area occupation rate of wirings arranged in an area of a planar region of said pad and formed under said pad is at least 50% of said area. This claim distinguishes patentably from the prior art relied upon in the rejections, as is apparent from the

discussion of Claim 1 vis-à-vis the prior art. The same remarks apply to new independent Claims 52 and 61. These claims and the claims dependent thereon should be allowed.

Although paragraph 2 on page 2 of the Office Action acknowledges Applicants' traversal of the requirement for election of species, the Office Action does not address Applicants' arguments in support of the traversal. It is respectfully submitted that all of the claims now presented, excepting the non-elected method Claims 16-35, should be examined.

The Commissioner is hereby authorized to charge to Deposit Account No. 50-1165 any fees under 37 C.F.R. §§ 1.16 and 1.17 that may be required by this paper and to credit any overpayment to that Account. If any extension of time is required in connection with the filing of this

paper and has not been requested separately, such extension is hereby requested.

Respectfully submitted,

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